PCI2361

User's Manual

Beijing ART Technology Development Co., Ltd.

Contents

Chapter 1 Overview

PCI2361 can be widely used in count, timing, frequency measurement, frequency occurrence, digital control, especially in the count, frequency measurement fields can be flexible and convenient combination to meet the different needs of a variety of users. The channel 0 provide positive/reverse output, you can easily control the GATE of the other channels, in order to facilitate frequency measurement applications.

Unpacking Checklist

Check the shipping carton for any damage. If the shipping carton and contents are damaged, notify the local dealer or sales for a replacement. Retain the shipping carton and packing material for inspection by the dealer.
Check for the following items in the package. If there are any missing items, contact your local dealer or sales.

- PCI2361 Data Acquisition Board
- ART Disk
  a) user's manual (pdf)
  b) drive
  c) catalog
- Warranty Card

FEATURES

Counter/Timer

- PCI2361 board has nine independent counter / timer
- Counter / timer CLK (clock input), GATE (gate), OUT (output), are all external. The GATE input with internal pull-up resistor to facilitate counting applications, and CLK, OUT terminals is the standard TTL electrical characteristics. Input low level is less than 0.4V, high level is greater than 2.6V, and the maximum output drive current of 1 OUT is mA.
- The counter 0 provide OUT forward and reverse output. (Reverse output is used to gate of the other channels' GATE), channel 0 output drive capability is 6 mA, TTL level.
- PCI2361 board provides two frequency clock outputs CLKOUT, one is 0.5μs, another one is 64μs, they can be selected by the XF3, clock output level is the TLL level, and drive capability is 6 mA.

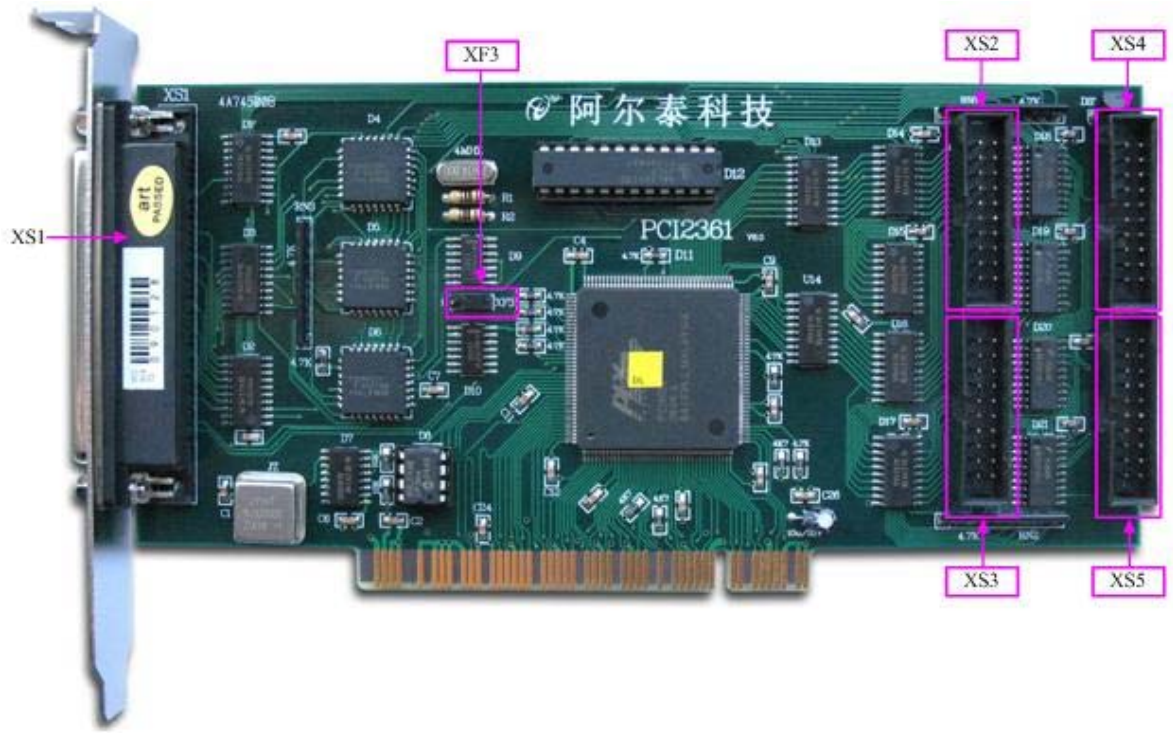
Digital Input/Output

- 32-ch digital input32-ch is digital output
- Electric Standard: TTL compatible
- Inhaled Current: <0.5mA
- Output TTL pull-down current: <20mA
- Output TTL pull-up current: <2.6mA

Board Dimension: 177.93mm (L) * 81.53mm (W) * 18.50mm (H)

Chapter 2 Components Layout Diagram and a Brief Description

2.1 The Main Component Layout Diagram



XS1: Signal input/output connector
XS2, XS3: Digital input port
XS4, XS5: Digital output port

2.2 Jumper

XF3: The jumper is set to internal clock output (CLKOUT) frequency, 1-2 shorted, the CLKOUT clock is 4MHz, 2 times divide-frequency of the onboard clock (the cycle is 0.5 microseconds), 2-3 shorted, the CLKOUT clock is 4MHz 256 times divide-frequency of the onboard clock (the cycle is 64 microseconds).

2.3 Signal Input and Output Connectors

2.3.1 37 core plug on the XS1 pin definition

Pin definition

Pin No.	Signal Name	Definition	Pin No.	Signal Name	Definition
1	CLKOUT	Clock Source Output	20	GATE0	Counter 0 Gate
2	OUT0	Counter 0 Output	21	NOUT0	Counter 0 Inverted Output
3	ClK1	Counter 1 Input	22	GATE1	Counter 1 Gate
4	OUT1	Counter 1 Output	23	CLK2	Counter 2 Output
5	GATE2	Counter 2 Gate	24	OUT2	Counter 2 Output
6	CLK3	Counter 3 Input	25	GATE3	Counter 3 Gate
7	OUT3	Counter 3 Output	26	CLK4	Counter 4 Input
8	GATE4	Counter 4 Gate	27	OUT4	Counter 4 Output
9	CLK5	Counter 5 Input	28	GATE5	Counter 5 Gate
10	OUT5	Counter 5 Output	29	CLK6	Counter 6 Input
11	GATE6	Counter 6 Gate	30	OUT6	Counter 6 Output
12	CLK7	Counter 7 Input	31	GATE7	Counter 7 Gate
13	OUT7	Counter 7 Output	32	CLK8	Counter 8 Input
14	GATE8	Counter 8 Gate	33	OUT8	Counter 8 Output
15	DGND	Digital Ground	34	DGND	Digital Ground
16	DGND	Digital Ground	35	DGND	Digital Ground
17	NC	Unconnected	36	NC	Unconnected
18	NC	Unconnected	37	VCC	+5V
19	VCC	+5V			

Notes: CLKx is the count pulse which is outputted to 8254 counter, GATEx is the corresponding GATE, OUTx is the output signal of 8254. The plus output of CLKOUT is the board's internal clock, its frequency can be setted by XF3, it also can support clock source to other count channels. The CLK clock input of channel 0 is short-circuited to OUTCLK, does not require external input.

2.3.2 Digital Signal Input/Output Connectors

Digital Input:

Pin definition of XS2

Pin No.	Signal Name	Pin No.	Signal Name
1	DI0	2	DI1
3	DI2	4	DI3
5	DI4	6	DI5
7	DI6	8	DI7
9	DI8	10	DI9

11	DI10	12	DI11
13	DI12	14	DI13
15	DI14	16	DI15
17	DGND	18	DGND
19	DGND	20	DGND

Pin definition of XS3

Pin No.	Signal Name	Pin No.	Signal Name
1	DI16	2	DI1
3	DI18	4	DI3
5	DI20	6	DI5
7	DI22	8	DI7
9	DI24	10	DI9
11	DI26	12	DI11
13	DI28	14	DI13
15	DI31	16	DI15
17	DGND	18	DGND
19	DGND	20	DGND

DI0~DI31: digital input

DGND: digital ground

Digital Output:

Pin definition of XS4

Pin No.	Signal Name	Pin No.	Signal Name
1	DO0	2	DO1
3	DO2	4	DO3
5	DO4	6	DO5
7	DO6	8	DO7
9	DO8	10	DO9
11	DO10	12	DO11
13	DO12	14	DO13
15	DO14	16	DO15
17	DGND	18	DGND
19	DGND	20	DGND

Pin definition of XS5

Pin No.	Signal Name	Pin No.	Signal Name
1	DO16	2	DO1
3	DO18	4	DO3
5	DO20	6	DO5
7	DO22	8	DO7
9	DO24	10	DO9
11	DO26	12	DO11
13	DO28	14	DO13

15	DO31	16	DO15
17	DGND	18	DGND
19	DGND	20	DGND

DO0~DO31: Digital output

DGND: digital ground

2.4 Data definitions and register description

2.4.1 PCI mapping space

	Size	Function Definition
The first memory	00H--0ffH	Operate to this space can modify the section of the PCI configuration
The first space	00H--0ffH	The same to the first memory, may not operate to the space
The second space	00H—0ffH	Operate to this space can control the input and output of the PCI boards. (DI, DO, Counter)

2.4.2 Register

Register	Offset Address	Description
DICTRL0	0x80	Read-in DI0-DI15
DICTRL1	0x82	Read-in DI16-DI31
DOTRL0	0x80	Read-in DO0-DO15
DOTRL1	0x82	Read-in DO16-DO31
CHIP0_CNT0	0x88	The four registers correspond to the internal registers of the first 8254. Ch0--Ch2's access to these registers must be 16 bits operation, but high 8 bits should be shielded.
CHIP0_CNT1	0x8A	
CHIP0_CNT2	0x8C	
CHIP0_CRTL	0x8E	
CHIP1_CNT0	0x90	The four registers correspond to the internal registers of the second 8254. Ch3—Ch5's access to these registers must be 16 bits operation, but high 8 bits should be shielded.
CHIP1_CNT1	0x92	
CHIP1_CNT2	0x94	
CHIP1_CRTL	0x96	
CHIP2_CNT0	0x98	The four registers correspond to the internal registers of the third 8254. Ch6—Ch8's access to these registers must be 16 bits operation, but high 8 bits should be shielded.
CHIP2_CNT1	0x9A	
CHIP2_CNT2	0x9C	
CHIP2_CRTL	0x9E	

Register Details

DICTRL0: The register can only be read, each bit corresponds to the input status of the input port of the board.

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DI15	DI14	DI13	DI12	DI11	DI10	DI9	DI8	DI7	DI6	DI5	DI4	DI3	DI2	DI1	DI0

DICTRL1: The register can only be read, each bit corresponds to the input status of the input port of the board.

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DI31	DI30	DI29	DI28	DI27	DI26	DI25	DI24	DI23	DI22	DI21	DI20	DI19	DI18	DI17	DI16

DOCTRL0: The register can only be written, each bit corresponds to the output status of the output port of the board.

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DO15	DO14	DO13	DO12	DO11	DO10	DO9	DO8	DO7	DO6	DO5	DO4	DO3	DO2	DO1	DO0

DOCTRL1: The register can only be written, each bit corresponds to the output status of the output port of the board.

Bit15	Bit14	Bit13	Bit12	Bit11	Bit10	Bit9	Bit8	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0
DO31	DO30	DO29	DO28	DO27	DO26	DO25	DO24	DO23	DO22	DO21	DO20	DO19	DO18	DO17	DO16

Count Operation Registers

CHIP0_CNT0
CHIP0_CNT1
CHIP0_CNT2
CHIP0_CRTL

The four registers correspond to the internal registers of the 8254 chip, they are 8-bit registers. But when visit them through the PCI interface; use 16-bit visit can get the right results, and the low 8 bits is valid.

High 8bit	Low 8bit
Invalid	Correspond to the internal registers of the 8254

CHIP1_CNT0
CHIP1_CNT1
CHIP1_CNT2
CHIP_CRTL

CHIP2_CNT0
CHIP2_CNT1
CHIP2_CNT2
CHIP3_CRTL

CHIP0xxxx correspond to ch0--ch2, CHIP1xxxx correspond to ch3--ch5, CHIP2xxxx correspond to ch6—ch8.

Chapter 3 Components Layout Diagram and a Brief Description

3.1 Control Word

Write control word and initial value to the 8254 internal control word register before use the 8254 internal counter.
Control word register format:

D7	D6	D5	D4	D3	D2	D1	D0
SC1	SC0	RL1	RL0	M2	M1	M0	BCD

BCD: Count mode, binary or BCD code.
M2, M1, M0: Counter work mode, there are 6 modes can be selected.
RL1, RL0: Register read/write operation length selected.
SC1, SCO: Register selected.

M2	M1	M0	Mode
0	0	0	0
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5

	Count Type
0	Binary Counter
1	Binary Code Decimal (BCD) Counter

RL1	RL0	Operate Type
0	0	Counter Latch Command
0	1	Read/write least significant byte only
1	0	Read/write most significant byte only
1	1	Read/write least significant byte first, then most significant byte.

SC1	SC0	Counter
0	0	Select Counter 0
0	1	Select Counter 1
1	0	Select Counter 2
1	1	Illegal

When the control word D0=0, it is binary count, the initial value can be chosen between 0000H and FFFFH. When the

control word D0=1, it is decimal count, the initial value can be chosen between 0000 and 9999. But the count value is always the maximum when the initial value is 0000.

3.2 Work Mode

MODE 0 Interrupt on terminal count

Mode 0 is typically used for event counting. After the Control Word is written, OUT is initially low, and will remain low until the Counter reaches zero. OUT then goes high and remains high until a new count or a new Mode 0 Control Word is written into the Counter.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After the Control Word and initial count are written to a Counter, the initial count will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not go high until N+1 CLK pulses after the initial count is written.

If a new count is written to the Counter, it will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte disables counting. OUT is set low immediately (no clock pulse required)
2) Writing the second byte allows the new count to be loaded on the next CLK pulse

This allows the counting sequence to be synchronized by software. Again , OUT does not go high until N+1 CLK pulses after the new count of N is written.

If an initial count is written while GATE=0, it will still be loaded on the next CLK pulse. When GATE goes high, OUT will go high N CLK pulse later, no CLK pulse is needed to load the Counter as this has already been done.

MODE 1 Hardware retriggerable one-shot

OUT will be initially high. OUT will go low on the CLK pulse following a trigger to begin the one-shot pulse, and will remain low until the Counter reaches zero.
OUT will then go high and remain high until the CLK pulse after the next trigger.

After writing the Control Word and initial count, the Counter is armed. A trigger results in loading the Counter and setting OUT low on the next CLK pulse, thus starting the one-shot pulse. An initial count of N will result in a one-shot pulse N CLK cycles in duration. The one-shout is retriggerable, hence OUT will remain low for N CLK pulses after any trigger. The one-shot pulse can be repeated without rewriting the same count into the counter. GATE has no effect on OUT.
If a new count is written to the Counter during a one-shot pulse, the current one-shot is not affected unless the counter is retriggered. In that case, the Counter is loaded with the new count and the one-shot pulse continues until the new count expires.

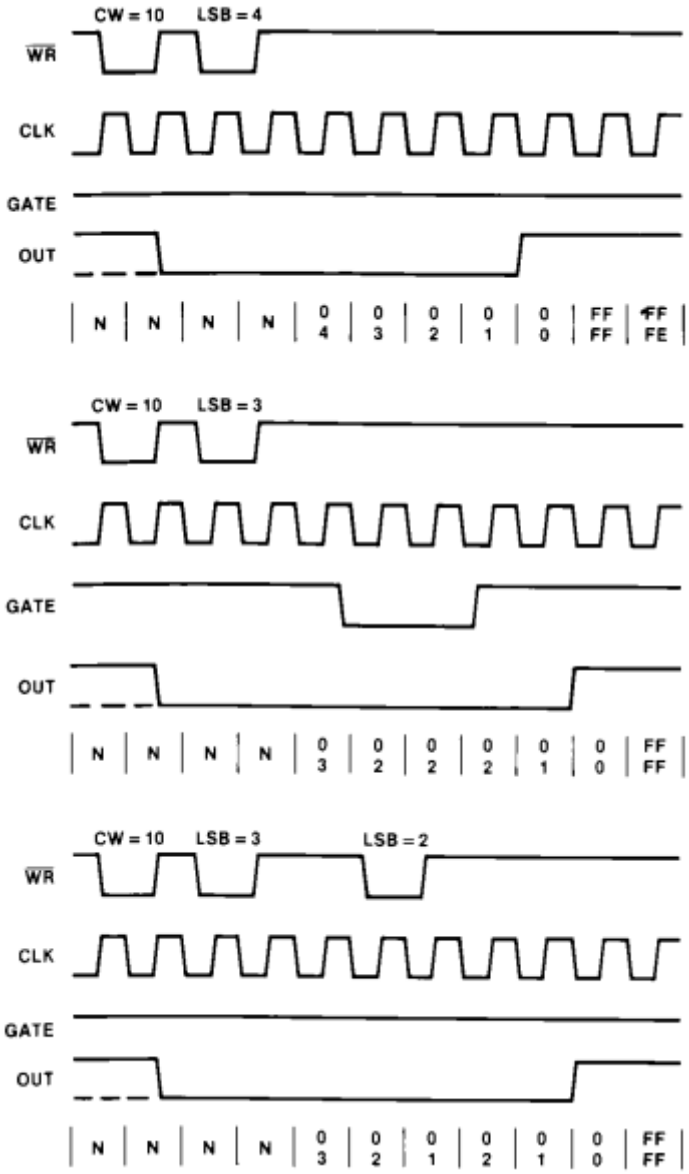


Figure 3.1 Mode 0

NOTE

The following conventions apply to all mode timing diagrams

1. Counters are programmed for binary (not BCD) counting and for reading/writing least significant byte (LSB) only.

2. The counter is always selected ($\overline{CS}$ always low) ***错误！未指定书签。***

3. CW stands for "Control Word"; CW=10 means a control word of 10 HEX is written to the counter.

4. LSB stands for "Least Significant Byte" of count.

5. Numbers below diagrams are count values. The lower number is the least significant byte. The upper number is the most significant byte.

Since the counter is programmed to read/writer LSB only, the most significant byte cannot be read.

N stands for an undefined count.

Vertical lines show transitions between count values.

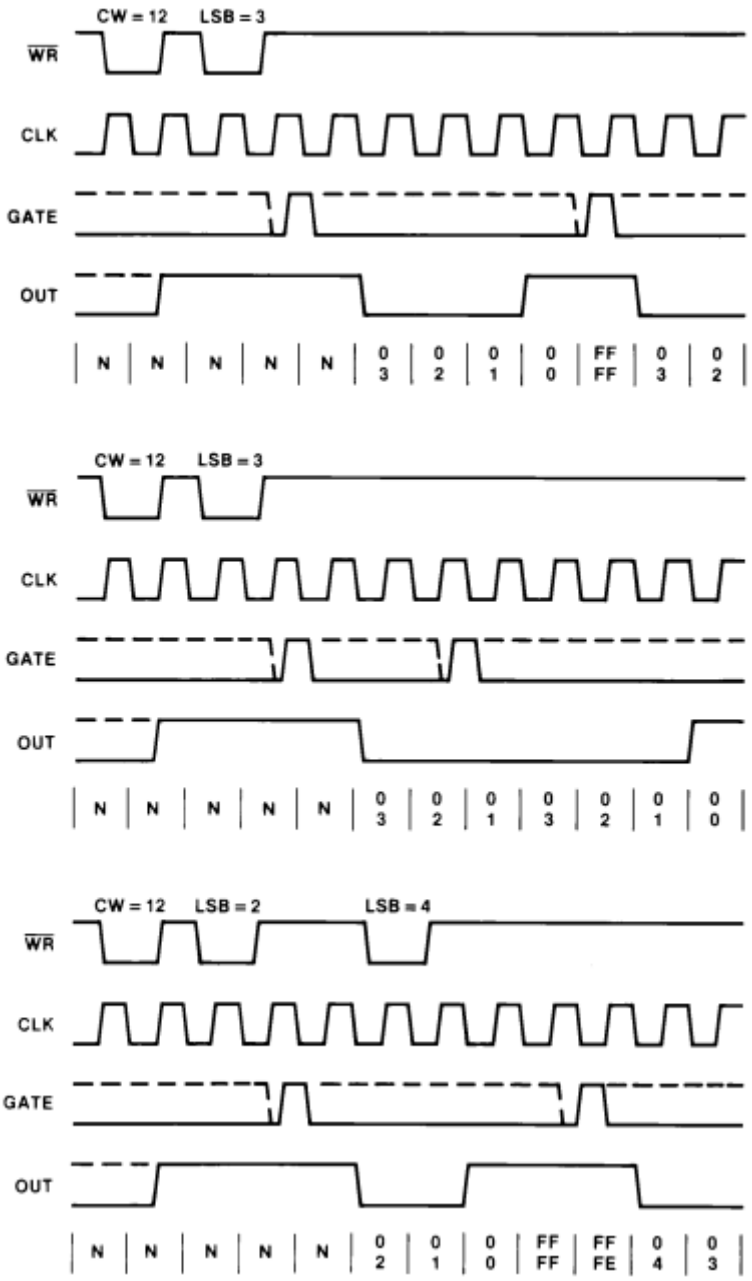


Figure 3.2 Mode 1

MODE 2 Rate Generator

This Mode functions like a divide-by-N counter. It is typically used to generate a Real Time Clock interrupt. OUT will initially be high. When the initial count has decremented to 1, OUT goes low for on CLK pulse. OUT then goes high again, the Counter reloads the initial count and the process is repeated. Mode 2 is periodic; the same sequence is repeated indefinitely. For an initial count of N, the sequence repeats every N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low during an output pulse, OUT is set high immediately. A trigger reloads the Counter with the initial count on the next CLK pulse; OUT goes low N CLK pulses after the trigger. Thus the GATE input can be used to synchronize the Counter.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. OUT goes low N CLK Pulses after the initial count is written. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current period, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new count will be loaded at the end of the current counting cycle. In mode2, a COUNT of 1 is illegal.

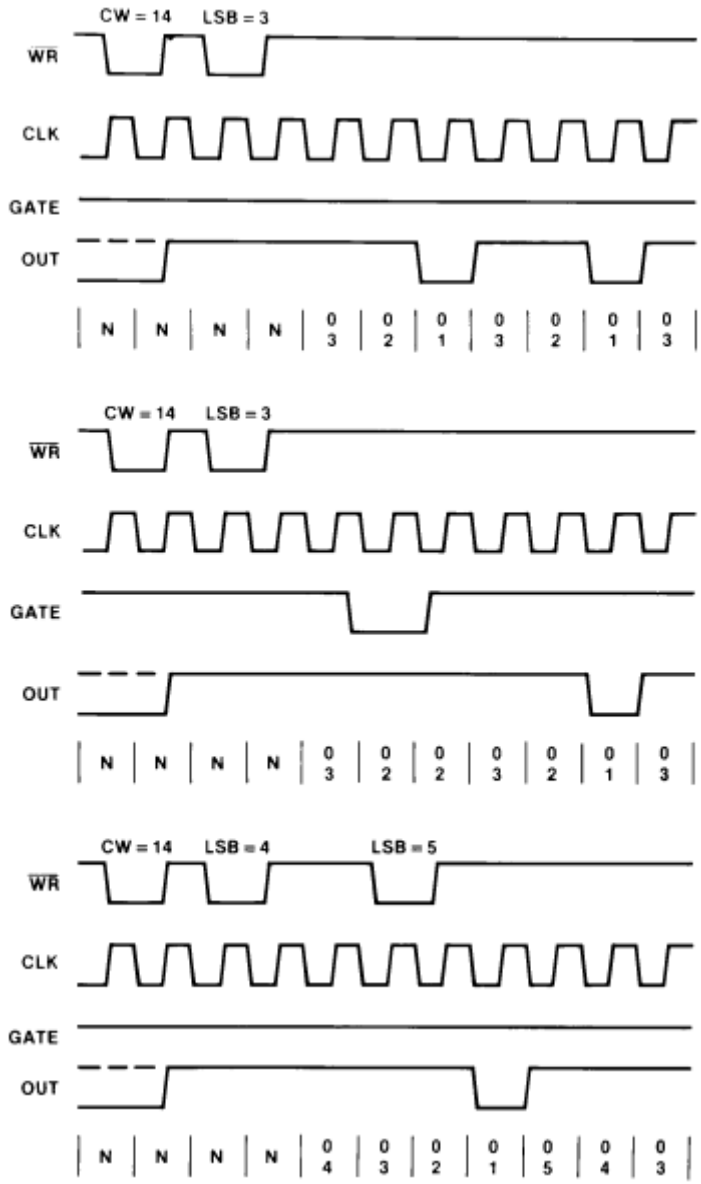


Figure 3.3 Mode 2

Note: A GATE transition should not occur one clock prior to terminal count.

MODE 3 Square wave mode

Mode 3 is typically used for Baud rate generation. Mode 3 is similar to Mode 2 except for the duty cycle of OUT. OUT will initially be high. When half the initial count has expired, OUT goes low for mainder of the count. Mode 3 is periodic; the sequence above is repeated indefinitely. An initial count of N results in a square wave with a period of N CLK cycles.

GATE=1 enables counting; GATE=0 disables counting. If GATE goes low while OUT is low, OUT is set high immediately; no CLK pulse is required. A trigger reloads the Counter with the initial count on the next CLK pulse. Thus

the GATE input can be used to synchronize the Counter

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This allows the Counter to be synchronized by software also.

Writing a new count while counting does not affect the current counting sequence. If a trigger is received after writing a new count but before the end of the current half-cycle of the square wave, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from the new count. Otherwise, the new counter will be loaded at the end of the current half-cycle.

Mode 3 is implemented as follows:

Even counts: OUT is initially high. The initial count is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. When the count expires OUT changes value and the Counter is reloaded with the initial count. The above process is repeated indefinitely.
Odd counts: OUT is initially high. The initial count minus one (an even number) is loaded on one CLK pulse and then is decremented by two on succeeding CLK pulses. One CLK pulse after the count expires. OUT goes low and the Counter is reloaded with the initial count minus one. Succeeding CLK pulses decrement the count by two. When the count expires, OUT goes high again and the Counter is reloaded with the initial count minus one. The above process is repeated indefinitely. So for odd counts, OUT will be high for (N+1)/2 counts and low for (N-1)/2 counts.

MODE 4 Software triggered strobe

OUT will be initially high. When the initial count expires, OUT will go low for one CLK pulse and then go high again. The counting sequence is “triggered” by writing the initial count.

GATE=1 enables counting; GATE=0 disables counting. GATE has no effect on OUT.

After writing a Control Word and initial count, the Counter will be loaded on the next CLK pulse. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+1 CLK pulses after the initial count is written.

If a new count is written during counting, if will be loaded on the next CLK pulse and counting will continue from the new count. If a two-byte count is written, the following happens:
1) Writing the first byte has no effect on counting.
2) Writing the second byte allows the new count to be loaded on the next CLK pulse.
This allows the sequence to be ‘‘retriggered’ by software. OUT strobe low N+1 CLK pulses after
the new count of N is written.

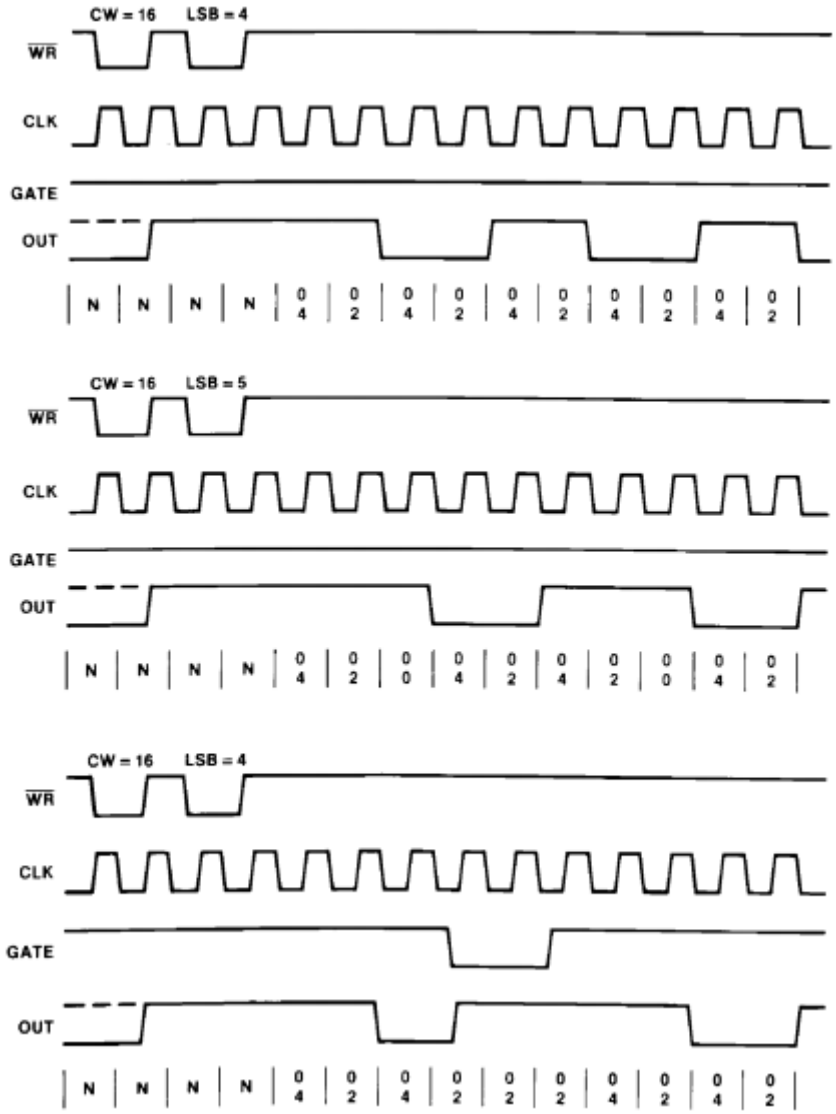


Figure 3.4 Mode 3

Note: A GATE transition should not occur one clock prior to terminal count.

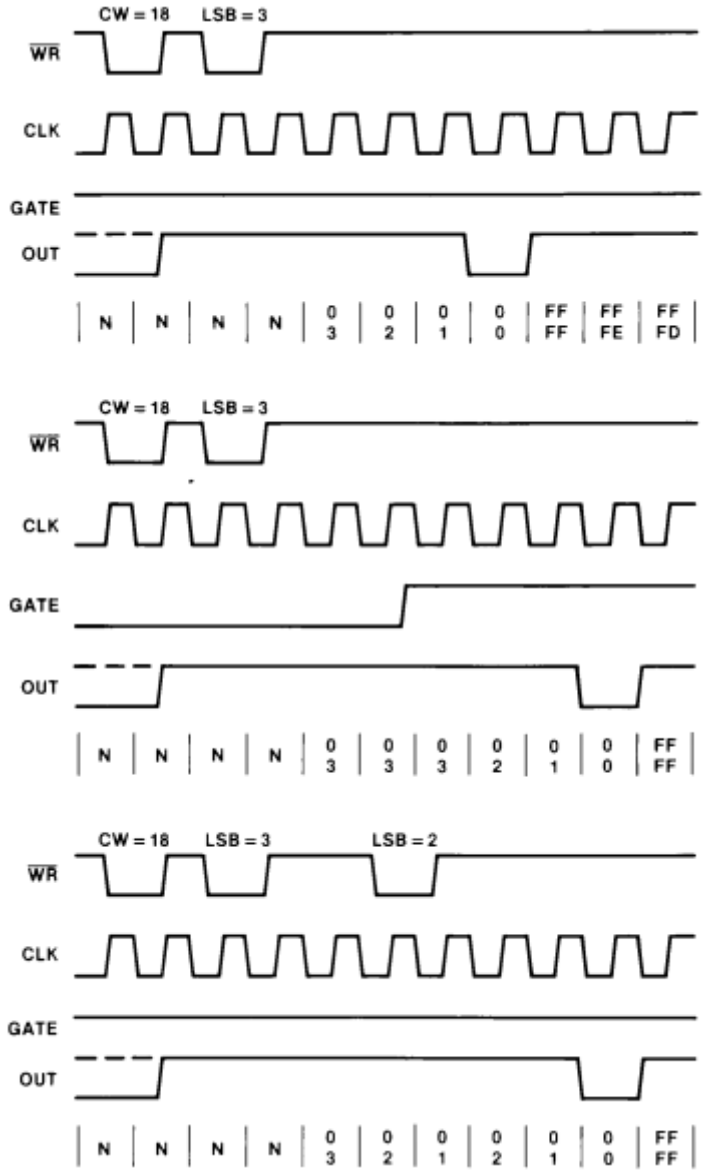


Figure 3.5 Mode 4

MODE 5 Hardware triggered strobe

OUT will initially be high. Counting is triggered by a rising edge of GATE. When the initial count has expired, OUT will go low for one CLK pulse and then go high again.

After writing the Control Word and initial count, the counter will not be loaded until the CLK pulse after a trigger. This CLK pulse does not decrement the count, so for an initial count of N, OUT does not strobe low until N+ 1 pulse after a trigger.

A trigger results in the Counter being loaded with the initial count on the next CLK pulse. The counting sequence is retriggerable. OUT will not strobe low for N+1 CLK pulses after any trigger. GATE has no effect on OUT.
If a new count is written during counting, the current counting sequence will not be affected. If a trigger occurs after the new count is written but before the current count expires, the Counter will be loaded with the new count on the next CLK pulse and counting will continue from there.

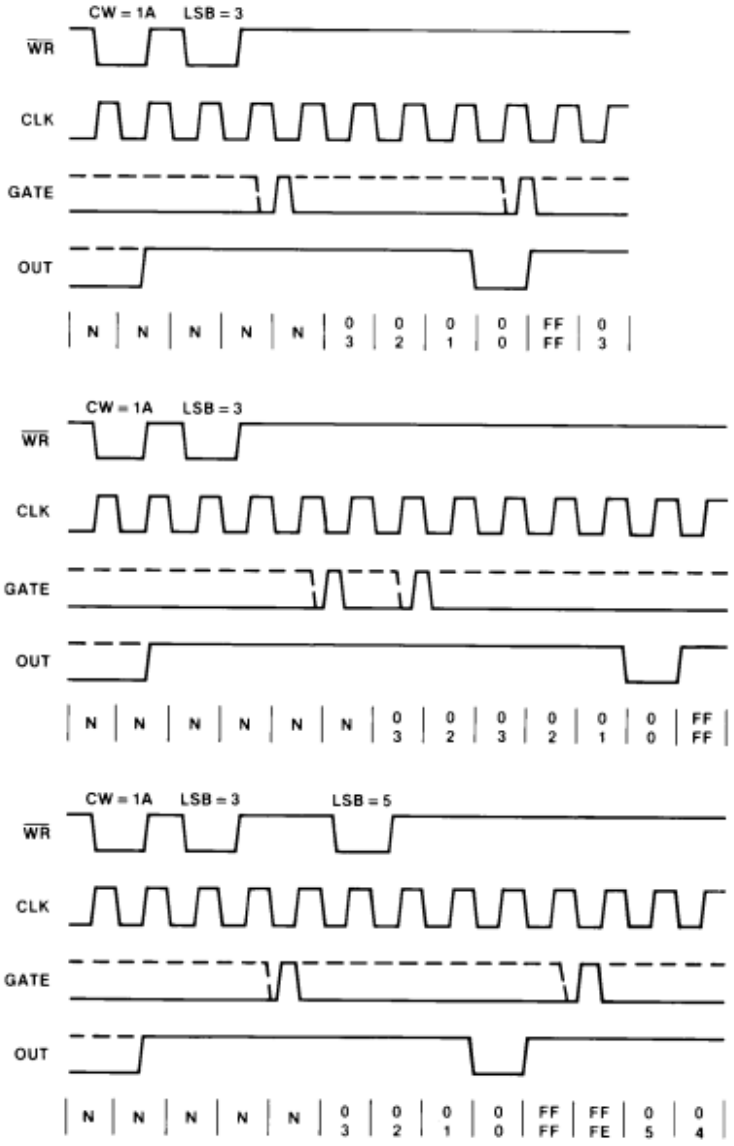


Figure 3.6 Mode 5

GATE Pin Operations Summary:

GATE	Low level or Falling edge	Rising edge	High level
Mode 0	Disables Counting	--	Enables Counting
Mode 1	- -	1. Initiates Counting 2. Resets Output after Next Clock	--
Mode 2	1) Disables Counting 2) Sets Output Immediately High	Initiates Counting	Enables Counting
Mode 3	2) Disables Counting 3) Sets Output Immediately High	Initiates Counting	Enables Counting
Mode 4	Disables Counting	--	Enables Counting
Mode 5	--	Initiates Counting	--

Note: each timer/counter of 8254 can not set the initial value to “1” in all operating modes, for the timer/counter will stop counting and output.

Chapter 4 Notes and Warranty Policy

4.1 Notes

In our products' packing, user can find a user manual, a PCI2361 module and a quality guarantee card. Users must keep quality guarantee card carefully, if the products have some problems and need repairing, please send products together with quality guarantee card to ART, we will provide good after-sale service and solve the problem as quickly as we can.

When using PCI2361, in order to prevent the IC (chip) from electrostatic harm, please do not touch IC (chip) in the front panel of PCI2361 module.

4.2 Warranty Policy

Thank you for choosing ART. To understand your rights and enjoy all the after-sales services we offer, please read the following carefully.

1. Before using ART's products please read the user manual and follow the instructions exactly. When senDOng in damaged products for repair, please attach an RMA application form which can be downloaded from: www.art-control.com.

2. All ART products come with a limited two-year warranty:

- The warranty period starts on the day the product is shipped from ART's factory
- For products containing storage devices (hard drives, flash cards, etc.), please back up your data before senDOng them for repair. ART is not responsible for any loss of data.
- Please ensure the use of properly licensed software with our systems. ART does not condone the use of pirated software and will not service systems using such software. ART will not be held legally responsible for products shipped with unlicensed software installed by the user.

3. Our repair service is not covered by ART's guarantee in the following situations:

- Damage caused by not following instructions in the User's Manual.
- Damage caused by carelessness on the user's part during product transportation.
- Damage caused by unsuitable storage environments (i.e. high temperatures, high humiDOty, or volatile chemicals).
- Damage from improper repair by unauthorized ART technicians.
- Products with altered and/or damaged serial numbers are not entitled to our service.

4. Customers are responsible for shipping costs to transport damaged products to our company or sales office.

5. To ensure the speed and quality of product repair, please download an RMA application form from our company website.

Products Rapid Installation and Self-check

Rapid Installation

Product-driven procedure is the operating system adaptive installation mode. After inserting the DOsc, you can select the appropriate board type on the pop-up interface, click the button【driver installation】; or select CD-ROM drive in Resource Explorer, locate the product catalog and enter into the APP folder, and implement Setup.exe file. After the installation, pop-up CD-ROM, shut off your computer, insert the PCI card. If it is a USB product, it can be DOrectly inserted into the device. When the system prompts that it finds a new hardware, you do not specify a drive path, the operating system can automatically look up it from the system DOrectory, and then you can complete the installation.

Self-check

At this moment, there should be installation information of the installed device in the Device Manager (when the device does not work, you can check this item.). Open "Start -> Programs -> ART Demonstration Monitoring and Control System -> CorresponDOng Board -> Advanced Testing Presentation System", the program is a standard testing procedure. Based on the specification of Pin definition, connect the signal acquisition data and test whether AD is normal or not. Connect the input pins to the corresponDOng output pins and use the testing procedure to test whether the switch is normal or not.

Delete Wrong Installation

When you select the wrong drive, or viruses lead to driver error, you can carry out the following operations: In Resource Explorer, open CD-ROM drive, run Others-> SUPPORT-> PCI.bat procedures, and delete the hardware information that relevant to our boards, and then carry out the process of section I all over again, we can complete the new installation.